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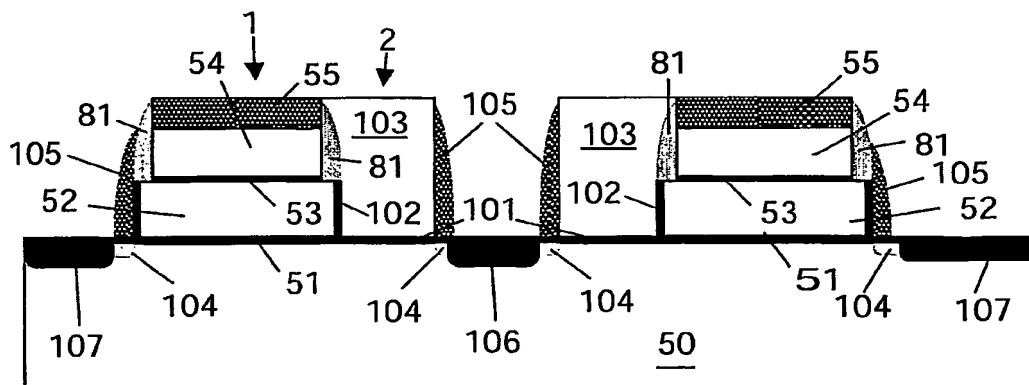
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(54) Title: 2-TRANSISTOR MEMORY CELL AND METHOD FOR MANUFACTURING



(57) Abstract: The present invention provides a method of manufacturing on a substrate (50) a 2-transistor memory cell comprising a storage transistor (1) having a memory gate stack (1) and a selecting transistor, there being a tunnel dielectric layer (51) between the substrate (50) and the memory gate stack. (1). The method comprises forming the memory gate stack (1) by providing a first conductive layer (52) and a second conductive layer (54) and etching the second conductive layer (54) thus forming a control gate and etching the first conductive layer (52) thus forming a floating gate. The method is characterized in that it comprises, before etching the first conductive layer (52), forming spacers (81) against the control gate in the direction of a channel to be formed under the tunnel dielectric layer (51), and thereafter using the spacers (81) as a hard mask to etch the first conductive layer (52) thus forming the floating gate, thus making the floating gate self aligned with the control gate. The present invention also provides a memory cell wherein the control gate (54) is smaller than the floating gate (52), and spacers (81) are present next to the control gate (54).

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